

*Application*  
*For*  
*United States Non-Provisional Utility Patent*

**INTEGRATED OPTICAL AND ELECTRONIC DEVICES**

*Inventors:*

**Lawrence C. Gunn III, 1008 East Palm Street, Altadena, CA 91001, a citizen of the United States.**

**Thierry J. Pinguet, 159 North Marengo Avenue, #304, Pasadena, CA 91101, a citizen of France.**

**Maxime Jean Rattier, 300 East Bellevue Drive, #331, Pasadena, CA 91101, a citizen of France.**

**Zhen-Li Ji, 679 Earlham Street, Pasadena, CA 91101, a citizen of Canada.**

**Jeremy Witzens, 130 S. Michigan Avenue, Pasadena, CA 91106, a citizen of Germany.**

## INTEGRATED OPTICAL AND ELECTRONIC DEVICES

### CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority from U.S. Provisional applications No. 60/391,278 filed June 24, 2002, 60/393,489 filed July 3, 2002, 60/393,490 filed July 3, 2002, 60/393,485 filed July 3, 2002, 60/393,683 filed July 3, 2002 and 60/393,682 filed July 3, 2002.

### FIELD OF THE INVENTION

The present invention relates to a method for the production of optical and electronic devices on the same monolithic integrated circuit.

### BACKGROUND OF THE INVENTION

The rapid expansion in the use of the Internet has resulted in a demand for high speed communications links and devices, including optical links and devices. Optical links using fiber optics have many advantages compared to electrical links: large bandwidth, high noise immunity, reduced power dissipation and minimal crosstalk. Optoelectronic integrated circuits made of silicon are highly desirable since they could be fabricated in the same foundries used to make VLSI integrated circuits. Optical devices integrated with their associated electronic circuits can eliminate the need for more

expensive hybrid optoelectronic circuits. Optical devices built using a standard CMOS process are very desirable for many reasons: high yields, low fabrication costs and continuous process improvements.

## SUMMARY OF THE INVENTION

One embodiment of the present invention is a method of using a standard CMOS process to fabricate optical and electronic devices at the same time on a monolithic integrated circuit. Optical devices such as waveguides, couplings, gratings, modulators, filters, multiplexers, demultiplexers, photodetectors and other optical devices can be made in a CMOS process at the same time as electronic devices are formed on the same integrated circuit. Many of the process steps and materials used in the production of CMOS circuits can be used to form elements of optical devices.

## BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross sectional view of a waveguide and a CMOS transistor, according to one embodiment of the present invention.

Figure 1A is a table summarizing the elements of the waveguide and the CMOS transistor of Figure 1, formed from the same materials at the same time on the same substrate.

Figure 2 is a cross sectional view of a strip loaded waveguide and a CMOS transistor, according to one embodiment of the present invention.

Figure 2A is a table summarizing the elements of the waveguide and the CMOS transistor of Figure 2 formed from the same materials at the same time on the same substrate.

Figure 3 is a cross sectional view of a strip loaded waveguide, according to another embodiment of the present invention.

Figure 3A is a table summarizing the elements of the waveguide of Figure 3 and the CMOS transistor of Figure 1, formed from the same materials at the same time on the same substrate.

Figure 4 is a side view of a waveguide with a light scattering element, according to one embodiment of the present invention.

Figure 4A is a table summarizing the elements of the waveguide and light scattering element of Figure 4 and the CMOS transistor of Figure 1, formed from the same materials at the same time on the same substrate.

Figure 5 is a side view of a waveguide with multiple light scattering elements, according to one embodiment of the present invention.

Figure 5A is a table summarizing the elements of the waveguide and the multiple light scattering elements of Figure 5 and the CMOS transistor of Figure 1, formed from the same materials at the same time on the same substrate.

Figure 6 is a side view of a strip loaded waveguide with a light scattering element, according to one embodiment of the present invention.

Figure 6A is a table summarizing the elements of the waveguide and light scattering element of Figure 6 and the CMOS transistor of Figure 1, formed from the same materials at the same time on the same substrate.

Figure 7 is a side view of a waveguide with a light scattering element, according to one embodiment of the present invention.

Figure 7A is a table summarizing the elements of the waveguide and light scattering element of Figure 7 and the CMOS transistor of Figure 1, formed from the same materials at the same time on the same substrate.

Figure 8 is a side view of a strip loaded waveguide with a light scattering element, according to one embodiment of the present invention.

Figure 8A is a table summarizing the elements of the waveguide and light scattering element of Figure 8 and the CMOS transistor of Figure 1, formed from the same materials at the same time on the same substrate.

Figure 9 is a side view of a strip loaded waveguide with a light scattering element, according to another embodiment of the present invention.

Figure 9A is a table summarizing the elements of the waveguide and light scattering element of Figure 9 and the CMOS transistor of Figure 1, formed from the same materials at the same time on the same substrate.

Figure 10 is a side view of a strip loaded waveguide with a light scattering element, according to one embodiment of the present invention.

Figure 10A is a table summarizing the elements of the waveguide and light scattering element of Figure 10 and the CMOS transistor of Figure 1, formed from the same materials at the same time on the same substrate.

Figure 11 is a cross sectional view of an active waveguide, according to one embodiment of the present invention.

Figure 11A is a table summarizing the elements of the active waveguide of Figure 11 and the CMOS transistor of Figure 1, formed from the same materials at the same time on the same substrate.

Figure 12 is a cross sectional view of an active waveguide, according to another embodiment of the present invention.

Figure 12A is a table summarizing the elements of the active waveguide of Figure 12 and the CMOS transistor of Figure 1, formed from the same materials at the same time on the same substrate.

Figure 13 is a top view of a waveguide to waveguide coupler, according to an embodiment of the present invention.

Figure 14 is a block diagram summarizing the process of designing a metal and dielectric stack for an optoelectronic integrated circuit.

## DETAILED DESCRIPTION

Figure 1 is a cross sectional view, not to scale, of a waveguide and a CMOS transistor, according to one embodiment of the present invention. Optical waveguide 150 and CMOS transistor 160 are part of integrated circuit 100, which has been fabricated on substrate 40. Substrate 40 is made of dielectric layer 44, which is frequently referred to as buried oxide (BOX) and typically consists of silicon dioxide and silicon layer 43. On top of silicon dioxide layer 44 is silicon layer 45. Layers 45, 44 and 43 together form what is commonly referred to as a SOI (silicon on insulator) wafer, which is frequently used for the production of CMOS integrated circuits.

Waveguide 150 is made of silicon core 151 and surrounding layers of cladding. The silicon core 151 in a cross sectional view can have one of many possible shapes, such as those of a square, a rectangle, a trapezoid or other form. Silicon dioxide layer 44 functions as a bottom cladding for the core 151. Surrounding waveguide core 151 on both sides of it is a layer of sidewall passivation 1 and sections of field oxide 15, which serve as side claddings. Sidewall passivation can be formed by thermal oxidation of

silicon. Field oxide 15 is frequently referred to as FOX. Sidewall passivation layers 1 are made of dielectric material, and typically consist of silicon dioxide. Sidewall passivation made of silicon dioxide is typically formed by thermal oxidation of silicon. Sections of field oxide 15 are made of dielectric material, and typically consist of silicon dioxide.

On top of the silicon core 151 are dielectric layers 2, 3, 4 and 5, which function as top cladding. Layer 2 is an oxide spacer layer of dielectric material, typically silicon dioxide. Layer 3 is a salicide blocking layer of dielectric material, typically silicon nitride. Layer 4 is a contact punch-through layer of dielectric material, which can be deposited from a mixture of silicon, oxygen and nitrogen. Layer 5 is an inter-level dielectric (ILD) which can be made of multiple layers of dielectric material. An ILD like layer 5 was historically made of silicon dioxide, but now is more typically made of a low k dielectric, such as silicon carbon oxide.

Those skilled in the art of the fabrication of integrated circuits can use any of a variety of well known processing methods and techniques to form the elements and layers, such as: thermal growth of oxide layers, PECVD, TEOS and others.

Waveguide 150 can be referred to as a channel waveguide formed on substrate 40.

CMOS transistor 160 is made of many layers and elements, which form three sections: the source 162, the drain 163 and the gate 164. The source 162 and the drain 163 are formed in the silicon body 161 of transistor 160. The sides of silicon body 161 are covered by layers of sidewall passivation 1. The gate 164 is made of many layers and elements formed on top of silicon body 161. Gate oxide layer 6 is formed on top of

silicon body 161. On top of gate oxide 6, polysilicon gate structure 9 is formed. The sides of the polysilicon gate 9 are covered by sidewall passivation layer 7 and dielectric layer 8. Gate oxide layer 6 and dielectric spacer 8 are typically made of silicon dioxide.

Silicon body 161 of transistor 160 can typically contain a well implant, which can be positively or negatively doped. Into two regions of silicon body 161 are placed extension implants 16. Source and drain implants 17 are also made into silicon body 161. The implants 16 and 17 are typically oppositely doped to the polarity of the well implant in the silicon body 161. A gate implant 17 is also made into polysilicon gate 9. A gate spacer for the polysilicon gate 9 is typically made of layers 8, 2 and 3. Layer 2 is an oxide spacer layer, typically made of silicon dioxide. Layer 3 is a salicide blocking layer, typically made of silicon nitride. Masking layers are designed to exclude implants from the waveguide 150.

Ohmic contacts 18, typically of cobalt silicide, are made into the doped regions of the transistor 160. After the ohmic contacts 18 have been formed, then layer 4, which is a contact punch-through layer, can be deposited. On top of layer 4, layer 5 is deposited. Layer 5 is an inter-level dielectric (ILD) which can be made of multiple layers of dielectric material. Coming through layers 4 and 5 are conductive plugs 19, typically made of tungsten, which connect the ohmic contacts 18 to the first metal layer 21.

First metal layer 21 (M1) is typically made of copper and connects to the conductive plugs 19 from the transistor and provides electrical connections to other circuits on the integrated circuit 100. Insulating the metal segments from each other in first metal layer 21 are layers 22 and 23. Layer 22 is a contact punch-through layer made of dielectric material. Layer



23 is an inter-layer dielectric (ILD) spacer layer made of dielectric material, typically silicon dioxide or silicon carbon oxide.

Layers 24 and 25 are inter-level dielectrics (ILD) separating the first metal layer 21 from the second metal layer (M2) 31. Layer 24 is a contact punch-through layer made of dielectric material. Layer 25 is an inter-layer dielectric, which can be made of multiple layers of dielectric.

First metal layer 21 is connected to second metal layer 31 by via 26 made of metal, typically copper or aluminum. The metal segments in layer 31 are separated from each other by dielectric layers 32 and 33. Layer 32 is a contact punch-through layer, made of dielectric material. Layer 33 is an inter-layer dielectric (ILD) spacer layer, made of dielectric material.

Figure 1 does not show any other metal layers, which provide other electrical interconnection pathways between the devices on an integrated circuit and which would be on top of the two metal layers shown.

The dielectric materials used in the fabrication of the waveguide can include many dielectric elements used in the fabrication of a CMOS transistor, such as: an inter-layer dielectric film, a gate spacer, a salicide block, a dielectric spacer, a passivation film, an isolation dielectric and a field oxide.

The dielectric materials used to make a waveguide and a CMOS transistor can include the following:  $\text{SiO}_2$ ,  $\text{SiCOH}$ ,  $\text{SiCOF}$ ,  $\text{Si}_3\text{N}_4$ ,  $\text{SiON}$ , BPSG, TEOS and silicon-based materials including one or more of the following elements: oxygen, carbon, nitrogen, hydrogen, boron, phosphorus, fluorine and arsenic.

SOI (silicon on insulator) wafers, such as one made of layers 45, 44 and 43, are frequently used for the production of CMOS integrated circuits.

Many parts or elements of the waveguide 150 and the CMOS transistor 160 are made of the same materials and can be made at the same time during the fabrication of a monolithic CMOS integrated circuit.

Figure 1A is a table summarizing the elements of the waveguide and transistor of Figure 1 formed from the same materials at the same time on the same substrate.

Silicon layer 45 is used to form the silicon core 151 of waveguide 150 and the silicon body 161 of transistor 160. The fabrication of these silicon elements can be done at the same time during the fabrication of a monolithic CMOS integrated circuit.

Sidewall passivation layers 1 of waveguide 150 and sidewall passivation layers 1 of transistor 160 can be formed at the same time of the same dielectric material on the same substrate.

The field oxide 15 which surrounds the waveguide 150 and the transistor 160 can be formed at the same time from the same dielectric material on the same substrate.

Dielectric layers 2, 3, 4 and 5 can be used to form the cladding for the waveguide 150 and dielectric elements of the transistor 160 of the same dielectric materials at the same time on the same substrate.

One particularly advantageous aspect of the present invention is the use of salicide blocking layer 3, which is part of the standard CMOS process, as an element of the cladding of the waveguide 150. Ohmic contacts are typically used to make electrical connections with any devices or components which have been fabricated on an integrated circuit. Ohmic contacts are formed by depositing metallic cobalt silicide on those parts of an integrated circuit, where it is desired to have metallic contact regions.

Salicide blocking layer 3 is deposited on those parts of an integrated circuit, where it is necessary to prevent the deposition of cobalt silicide in subsequent process steps.

If cobalt silicide were deposited into the core of an optical waveguide, light would not be able to pass through that section of the waveguide. Thus, salicide blocking layer 3 is used to protect the core of an optical waveguide from the light blocking deposition of metallic cobalt silicide.

A particularly advantageous aspect of the present invention is the fabrication of the elements of a waveguide and the elements of a CMOS transistor at the same time and using the same materials on the same substrate, using standard CMOS processing steps.

Figure 2 is a cross sectional view, not to scale, of a strip loaded waveguide and a CMOS transistor, according to one embodiment of the present invention. Optical waveguide 250 and CMOS transistor 160 are part of integrated circuit 200, which has been fabricated on substrate 40. Substrate 40 is made of dielectric layer 44, which is typically silicon dioxide and silicon layer 43. On top of silicon dioxide layer 44 is silicon layer 45. Layers 45, 44 and 43 together form what is commonly referred to as a SOI (silicon on insulator) wafer, which is typically used for the production of CMOS integrated circuits.

Waveguide 250 is made of core 251 and surrounding layers of cladding. The core 251 is made of silicon slab 252, dielectric layer 6 and polysilicon strip 9. Dielectric layer 6 is typically made of silicon dioxide. Silicon dioxide layer 44 functions as a bottom cladding for the core 251. On the side of silicon slab 252 is a layer of sidewall passivation 1 and a section of field oxide 15, which serve as side claddings. Sidewall

passivation layer 1 is made of dielectric material, typically silicon dioxide. Sidewall passivation can be formed by thermal oxidation of silicon. Sections of field oxide 15 are made of dielectric material, typically silicon dioxide. On top of the core 251 are dielectric layers 2, 3, 4 and 5, which function as top cladding. Layer 2 is an oxide spacer layer of dielectric material, typically silicon dioxide. Layer 3 is a salicide blocking layer of dielectric material, typically silicon nitride. Layer 4 is a contact punch-through layer of dielectric material, which can be deposited from a mixture of silicon, oxygen and nitrogen. Layer 5 is an inter-level dielectric (ILD) which can be made of multiple layers of dielectric material.

CMOS transistor 160 is very similar to the CMOS transistor shown in Figure 1 and as previously described herein. The dielectric materials listed with respect to Figure 1 are all usable as dielectric materials for the devices shown in Figure 2.

SOI (silicon on insulator) wafers, such as one made of layers 45, 44 and 43, are frequently used for the production of CMOS integrated circuits. Many parts or elements of the waveguide 250 and the CMOS transistor 160 are made of the same materials and can be made at the same time during the fabrication of a monolithic CMOS integrated circuit.

Figure 2A is a table summarizing the elements of the waveguide and transistor of Figure 2 formed from the same materials at the same time on the same substrate.

Silicon layer 45 is used to form the silicon slab 252 of waveguide 250 and the silicon body 161 of transistor 160. These silicon elements can be formed of the same material at the same time during the fabrication of a monolithic CMOS integrated circuit.

Sidewall passivation layer 1 of waveguide 250 and sidewall passivation layers 1 of transistor 160 can be formed at the same time of the same dielectric material on the same substrate.

The field oxide 15 which surrounds the waveguide 250 and the transistor 160 can be formed at the same time from the same dielectric material on the same substrate.

Dielectric layer 6 of the waveguide 250 and the gate oxide 6 of the transistor 160 can be formed at the same time of the same dielectric material on the same substrate.

Polysilicon strip 9 of the waveguide 250 and the polysilicon gate 9 of the CMOS transistor 160 can be formed at the same time of the same dielectric material on the same substrate.

Sidewall passivation layers 7 of waveguide 250 and sidewall passivation layers 7 of CMOS transistor 160 of Figure 1 can be formed at the same time from the same dielectric material on the same substrate.

Dielectric layers 8 of waveguide 250 and the dielectric layers 8 of CMOS transistor 160 of Figure 1 can be formed at the same time from the same dielectric material on the same substrate.

Dielectric layers 2, 3, 4 and 5 used to form the cladding for the waveguide 250 and dielectric layers 2, 3, 4 and 5 of CMOS transistor 160 in Figure 1 can be formed at the same time of the same dielectric materials on the same substrate.

One particularly advantageous aspect of the present invention is the use of the salicide blocking layer 3, which is part of the standard CMOS process, as one of the layers of the cladding of the waveguide 250. The salicide blocking layer 3 is an essential layer in the CMOS process of

forming the ohmic contacts needed to make electrical connections to the transistor 160. The salicide blocking layer 3 prevents the deposition of cobalt silicide in any part of a CMOS integrated circuit, where it is not needed. If cobalt silicide is deposited into the core of an optical waveguide, light will not be able to pass through that section of the waveguide. Thus, salicide blocking layer 3 is essential to protecting the core of an optical waveguide from the light blocking deposition of metallic cobalt salicide.

In an alternate embodiment of the present invention, waveguide 250 is fabricated without dielectric layer 6, where the polysilicon strip 9 is formed on top of waveguide core 251.

A particularly advantageous aspect of the present invention is the fabrication of the elements of a waveguide and the elements of a CMOS transistor at the same time and using the same materials on the same substrate, using standard CMOS processing steps.

Figure 3 is a cross sectional view, not to scale, of a strip loaded waveguide, according to another embodiment of the present invention. Optical waveguide 350 is part of integrated circuit 300, which has been fabricated on substrate 50. Substrate 50 is made of dielectric layer 44, which is typically silicon dioxide, silicon layer 43, silicon dioxide layer 42 and silicon layer 41. On top of silicon dioxide layer 44 is silicon layer 45. Layers 45, 44, 43, 42 and 41 together form a wafer, and integrated optical and electronic devices can be formed on such a wafer using standard CMOS processes.

Waveguide 350 is made of a core 351 and surrounding layers of cladding. Core 351 is made of silicon layer 43, dielectric layer 44 and silicon strip 352. Silicon dioxide layer 42 functions as a bottom cladding for

the core 351. Surrounding silicon strip 352 on both sides of it is a layer of sidewall passivation 1 and sections of field oxide 15, which serve as side cladding. Sidewall passivation layers 1 are made of dielectric material, typically silicon dioxide. Sidewall passivation can be formed by thermal oxidation of silicon. Field oxide 15 is made of dielectric material, typically silicon dioxide.

On top of the core 351 are dielectric layers 2, 3, 4 and 5, which function as a top cladding. Layer 2 is an oxide spacer layer of dielectric material, typically silicon dioxide. Layer 3 is a salicide blocking layer of dielectric material, typically silicon nitride. Layer 4 is a contact punch-through layer of dielectric material, which can be deposited from a mixture of silicon, oxygen and nitrogen. Layer 5 is an inter-level dielectric (ILD) which can be made of multiple layers of dielectric material.

Waveguide 350 and a CMOS transistor, like the one discussed in detail with respect to Figure 1, can be fabricated on the same monolithic integrated circuit, in a manner similar to the way in which waveguide 150 and transistor 160 in Figure 1 were fabricated.

The dielectric materials listed with respect to Figure 1 are all usable as dielectric materials for the waveguide 350 shown in Figure 3.

Figure 3A is a table summarizing the elements of the waveguide of Figure 3 and the CMOS transistor of Figure 1 formed from the same materials at the same time on the same substrate.

Silicon layer 45 is used to form the silicon slab 351 of waveguide 350 and can be used to form the silicon body of a transistor in a CMOS process. The fabrication of these silicon elements can be done at the same time during the fabrication of a monolithic CMOS integrated circuit.

Sidewall passivation layers 1 of waveguide 350 and the sidewall passivation layers for the silicon body of a CMOS transistor can be formed at the same time of the same dielectric material on the same substrate.

Field oxide 15 surrounding silicon strip 352 and the field oxide surrounding the body of a CMOS transistor can be formed at the same time from the same dielectric material on the same substrate.

Dielectric layers 2, 3, 4 and 5, used to form the cladding for the waveguide 350 and dielectric layers 2, 3, 4 and 5 of CMOS transistor 160 in Figure 1 can be formed at the same time of the same dielectric materials on the same substrate.

In an alternate embodiment of the present invention, waveguide 350 is fabricated as a strip loaded waveguide with a dielectric layer on top of the waveguide core and with a polysilicon strip on the dielectric layer.

In another alternate embodiment of the present invention, waveguide 350 is fabricated as a strip loaded waveguide with a polysilicon strip on the waveguide core.

One particularly advantageous aspect of the present invention is the use of the salicide blocking layer 3, which is part of the standard CMOS process, as an element of the cladding of the waveguide 350. The salicide blocking layer 3 is an essential layer in the CMOS process of forming the ohmic contacts needed to make electrical connections to the transistor 160. The salicide blocking layer 3 prevents the deposition of cobalt silicide in any part of a CMOS integrated circuit, where it is not needed. If cobalt silicide is deposited into the core of an optical waveguide, light will not be able to pass through that section of the waveguide. Thus, salicide blocking layer 3



is essential to protecting the core of an optical waveguide from the light blocking deposition of metallic cobalt silicide.

A particularly advantageous aspect of the present invention is the fabrication of the elements of a waveguide and the elements of a CMOS transistor at the same time and using the same materials on the same substrate, using standard CMOS processing steps.

Figure 4 is a side view, not to scale, of a waveguide with a light scattering element, according to one embodiment of the present invention. Optical waveguide 450 and light scattering element 455 are part of integrated circuit 400, which has been fabricated on substrate 40. Substrate 40 is made of dielectric layer 44, which is typically silicon dioxide and silicon layer 43. On top of silicon dioxide layer 44 is silicon layer 45. Layers 45, 44 and 43 together form what is commonly referred to as a SOI (silicon on insulator) wafer, which is frequently used for the production of CMOS integrated circuits.

Waveguide 450 is made of silicon core 451 and surrounding layers of cladding. The silicon core 451 in a cross sectional view can have one of many possible shapes, such as those of a square, a rectangle, a trapezoid or other form. Silicon dioxide layer 44 functions as a bottom cladding for the core 451. Sidewall passivation layers and sections of field oxide, not shown in Figure 4, are made of dielectric materials and provide side cladding for the waveguide core 451. Sidewall passivation can be formed by thermal oxidation of silicon.

Light scattering element 455 is disposed on top of silicon core 451. Light scattering element 455 includes dielectric layer 6, polysilicon structure 9, sidewall passivation layers 7, dielectric layers 8 and surrounding cladding.

Dielectric layer 6, sidewall passivation layer 7 and dielectric layer 8 are typically made of silicon dioxide.

Polysilicon structure 9 in a cross sectional view can have one of many possible shapes, such as those of a square, a rectangle, a trapezoid or other form. The design of polysilicon structure 9, including its size and shape is dependent on the requirements of a particular application and is well known to those skilled in the art.

On top of the waveguide core 451 and the light scattering element 455 are dielectric layers 2, 3, 4 and 5, which provide top cladding for the waveguide core 451 and top and side cladding for light scattering element 455. Layer 2 is an oxide spacer layer of dielectric material, typically silicon dioxide. Layer 3 is a salicide blocking layer of dielectric material, typically silicon nitride. Layer 4 is a contact punch-through layer of dielectric material, which can be deposited from a mixture of silicon, oxygen and nitrogen. Layer 5 is an inter-level dielectric (ILD) which can be made of multiple layers of dielectric material. ILD layer 5 can be made of silicon dioxide or preferably, a low k dielectric, such as silicon carbon oxide.

Light 60 propagating through waveguide core 451 will be mainly confined to the core 451, primarily in a single mode, due to the large difference in refractive indices between the silicon core 451 and the surrounding claddings. The single mode distribution of light propagating in the core 451 is shown by graph 61, which shows that the peak power level of the light in the waveguide 450 is primarily near to the center of the core 451. Graph 61 is an approximate illustration of the distribution of power in the waveguide 450. The silicon core 451 has a refractive index ( $n$ ) of

approximately 3.5 as compared to a refractive index of about 1.5 for silicon dioxide, which is the primary material of the claddings.

As light 60 travels through the waveguide 450 it is primarily confined near to the center of the core, but some of the light is propagating through the cladding on top of the core. When the light in the top cladding reaches the boundary with the polysilicon structure 9 in the light scattering element 455, some of the light is scattered downward 63 and some is scattered upward 62. The scattering of light by the light scattering element 455 is primarily due to the abrupt change in refractive index at the boundary between the top cladding and the polysilicon 9. The top cladding layers 2, 3 and 4 are typically made of silicon dioxide, which has a refractive index of about 1.5. Polysilicon 9 has a refractive index of about 3.6. The light scattering element 455 provides an optical coupling between the core 451 and the layers above and below the core.

Light can also travel in the opposite direction through the light scattering element 455, so that light which is traveling down from a higher level can be coupled into the core of the waveguide by the light scattering element 455.

A typical integrated circuit 400 will have several metal layers above the dielectric layers 5 to provide for interconnections between the components fabricated on the same substrate, but these layers are not shown in Figure 4. For light to be scattered up out of waveguide 450 or for light to be coupled into waveguide 450 from above, there cannot be any segments or pieces of any metal layers directly above the light scattering element 455.

Many parts of the light scattering element 455 of Figure 4 and the CMOS transistor 160 of Figures 1 and 2 are made of the same materials and

can be made at the same time during the fabrication of a monolithic CMOS integrated circuit.

Figure 4A is a table summarizing the parts of the waveguide and light scattering element of Figure 4 and the CMOS transistor of Figure 1 formed from the same materials at the same time on the same substrate.

Silicon layer 45 is used to form the silicon core 451 and the silicon body 161 of CMOS transistor 160 of Figure 1. These silicon elements can be formed of the same material at the same time during the fabrication of a monolithic CMOS integrated circuit.

Sidewall passivation layers, not shown in Figure 4, on the sides of waveguide core 451 and the sidewall passivation layers 1 for the silicon body of CMOS transistor 160 in Figure 1 can be formed at the same time of the same dielectric material on the same substrate.

Field oxide sections, not shown in Figure 4, on the sides of silicon core 451 and the field oxide 15 surrounding the body of CMOS transistor 160 of Figure 1 can be formed at the same time from the same dielectric material on the same substrate.

Dielectric layer 6 of the light scattering element 455 and the gate oxide 6 of CMOS transistor 160 of Figure 1 can be formed at the same time of the same dielectric material on the same substrate.

Polysilicon strip 9 of the light scattering element 455 and the polysilicon gate 9 of CMOS transistor 160 of Figure 1 can be formed at the same time of the same dielectric material on the same substrate.

Sidewall passivation layers 7 of the light scattering element 455 and sidewall passivation layers 7 of CMOS transistor 160 of Figure 1 can be

formed at the same time from the same dielectric material on the same substrate.

Dielectric layers 8 of the light scattering element 455 and the dielectric layers 8 of CMOS transistor 160 of Figure 1 can be formed at the same time from the same dielectric material on the same substrate.

Dielectric layers 2, 3, 4 and 5 used to form the cladding for the waveguide 450 and the light scattering element 455 and dielectric layers 2, 3, 4 and 5 of CMOS transistor 160 in Figure 1 can be formed at the same time of the same dielectric materials on the same substrate.

In alternate embodiments of the present invention, light scattering element 455 is fabricated without dielectric layer 6, where the polysilicon strip 9 is on top of waveguide core 451.

One particularly advantageous aspect of the present invention is the use of the salicide blocking layer 3, which is part of the standard CMOS process, as an element of the cladding for the waveguide 450 and the light scattering element 455. The salicide blocking layer 3 is an essential layer in the CMOS process of forming the ohmic contacts needed to make electrical connections to the transistor 160. The salicide blocking layer 3 prevents the deposition of cobalt silicide in any part of a CMOS integrated circuit, where it is not needed. If cobalt silicide is deposited into the core of an optical waveguide, light will not be able to pass through that section of the waveguide. Thus, salicide blocking layer 3 is essential to protecting the core of an optical waveguide from the light blocking deposition of metallic cobalt silicide.

A particularly advantageous aspect of the present invention is the fabrication of the parts of a light scattering element and the parts of a CMOS

transistor at the same time and using the same materials on the same substrate, during standard CMOS processing steps.

Figure 5 is a side view, not to scale, of a waveguide and multiple light scattering elements, according to one embodiment of the present invention. Figure 5 includes optical waveguide 450 and light scattering elements 556, which are part of integrated circuit 400, and has been fabricated on substrate 40. Light scattering elements 556 are made of as many individual elements 455A, 455B, 455C, etc. as may be needed for a particular application, but only three are shown in Figure 5.

The size of each light scattering element 455A, etc. may or may not be identical, depending on the application for which they are designed, such as a grating coupler. The spacing between the light scattering elements can be periodic or not periodic, depending on the requirements of a specific application. Determining the best size and spacing of the elements of devices such as grating couplers is well known to those skilled in the art.

The materials and processing steps used to fabricate device 556 are the same ones described in detail with respect to Figure 4, except that Figure 5 has multiple scattering elements disposed on the silicon waveguide core 451.

The operation of light scattering elements 556 in Figure 5 is similar to the operation of light scattering element 455 in Figure 4. Light 61 propagating through the waveguide 450 is confined primarily to the core 451 as shown in the power distribution graph 60. As the light enters regions of the core 451 under the light scattering elements 455A, etc. some of the light is scattered upwards 62 and downwards 63. The light scattering elements

556 provides a coupling between the core 451 and the layers above and below the core.

Light can also travel in the opposite direction through the light scattering elements 556, so that light which is propagating down from a higher level can be coupled into the core of the waveguide by the multiple light scattering elements 556. The light incident from above on the light scattering elements 556 will be coupled into the waveguide 450. The light incident from above could be propagating through an optical fiber, for example, where the end of the optical fiber is placed in direct contact with the top layer of the integrated circuit, just above the light scattering elements 556.

A typical integrated circuit 400 will have several metal layers above the dielectric layers 5 to provide for interconnections between the components fabricated on the same substrate, but these layers are not shown in Figure 4. For light to be scattered up out of waveguide 450 or for light to be coupled into waveguide 450 from above, there cannot be any segments or pieces of any metal layers directly above the light scattering elements 556.

In alternate embodiments of the present invention, light scattering elements 556 are fabricated without dielectric layer 6.

As was discussed with respect to the light scattering element 455 in Figure 4, many parts of the light scattering elements 556 of Figure 5 and the CMOS transistor 160 of Figures 1 and 2 are made of the same materials and can be made at the same time during the fabrication of a monolithic CMOS integrated circuit.

Figure 5A is a table summarizing the parts of the waveguide and light scattering elements 556 of Figure 5 and the CMOS transistor of Figure 1 formed from the same materials at the same time on the same substrate.

One particularly advantageous aspect of the present invention is the use of the salicide blocking layer 3, which is part of the standard CMOS process, as a part of the cladding of the waveguide 450 and light scattering elements 556. The salicide blocking layer 3 is an essential layer in the CMOS process of forming the ohmic contacts needed to make electrical connections to the transistor 160. The salicide blocking layer 3 prevents the deposition of cobalt silicide in any part of a CMOS integrated circuit, where it is not needed. If cobalt silicide is deposited into the core of an optical waveguide, light will not be able to pass through that section of the waveguide. Thus, salicide blocking layer 3 is essential to protecting the core of an optical waveguide from the light blocking deposition of metallic cobalt silicide.

A particularly advantageous aspect of the present invention is the fabrication of parts of light scattering elements and parts of a CMOS transistor at the same time using the same materials on the same substrate, during standard CMOS processing steps.

Figure 6 is a side view, not to scale, of a strip loaded waveguide with a light scattering element, according to one embodiment of the present invention. Light scattering element 655 and optical waveguide 650 are part of integrated circuit 600, which has been fabricated on substrate 50. Substrate 50 is made of dielectric layer 44, which is typically silicon dioxide, silicon layer 43, silicon dioxide layer 42 and silicon layer 41. On top of silicon dioxide layer 44 is silicon layer 45. Layers 45, 44, 43, 42 and



41 together form a wafer, and integrated optical and electronic devices can be formed on such a wafer using standard CMOS processes.

Waveguide 650 is made of a core 651 and surrounding layers of cladding. Core 651 is made of silicon layer 43, dielectric layer 44 and silicon strip 652. Silicon dioxide layer 42 functions as a bottom cladding for the core 651. Surrounding silicon strip 652 on both sides of it is a layer of sidewall passivation 1 and sections of field oxide 15, which serve as side cladding. Sidewall passivation layers 1 and field oxide 15 are made of dielectric material, typically silicon dioxide. Sidewall passivation can be formed by thermal oxidation of silicon.

Light scattering element 655 is disposed on top of silicon core 651. Light scattering element 655 includes dielectric layer 6, polysilicon structure 9, sidewall passivation layers 7, dielectric layers 8 and surrounding cladding. Dielectric layer 6, sidewall passivation layer 7 and dielectric layer 8 are typically made of silicon dioxide.

Polysilicon structure 9 in a cross sectional view can have one of many possible shapes, such as those of a square, a rectangle, a trapezoid or other form. The size and shape of polysilicon structure 9 is dependent on the requirements of a particular application and is well known to those skilled in the art.

On top of the core 651 are dielectric layers 2, 3, 4 and 5, which function as a top cladding. Layer 2 is an oxide spacer layer of dielectric material, typically silicon dioxide. Layer 3 is a salicide block layer of dielectric material, typically silicon nitride. Layer 4 is a contact punch-through layer of dielectric material, which can be deposited from a mixture

of silicon, oxygen and nitrogen. Layer 5 is an inter-layer dielectric (ILD) which can be made of multiple layers of dielectric material.

The materials and processing steps used to fabricate light scattering element 655 are the same ones described in detail with respect to Figure 4, except that light scattering element 655 is fabricated on a different substrate.

The operation of light scattering element 655 in Figure 6 is similar to the operation of light scattering element 455 in Figure 4. Light 61 propagating through the waveguide 450 is confined primarily to the core 651 as shown in the power distribution graph 60. As the light enters regions of the core 651 under the light scattering elements 655, some of the light is scattered upwards 62 and downwards 63. The light scattering element 655 provides an optical coupling between the core 651 and the layers above and below the core.

Light can also travel in the opposite direction through the light scattering element 655, so that light which is propagating down from a higher level can be coupled into the core of the waveguide by light scattering element 655. The light incident from above on the light scattering element 655 can be coupled into the waveguide 650.

A typical integrated circuit 600 will have several metal layers above the dielectric layers 5 to provide for interconnections between the components fabricated on the same substrate, but these layers are not shown in Figure 6. For light to be scattered up out of waveguide 650 or for light to be coupled into waveguide 650 from above, there cannot be any segments or pieces of any metal layers directly above the light scattering element 655.

In alternate embodiments of the present invention, light scattering element 655 is fabricated without dielectric layer 6, so that polysilicon structure 9 is disposed on silicon waveguide core 651.

The dielectric materials listed herein with respect to Figure 1 are all usable as dielectric materials for the waveguide 650 shown in Figure 6.

As was discussed with respect to the light scattering element 455 in Figure 4, many parts or elements of the light scattering element 655 of Figure 6 and the CMOS transistor 160 of Figures 1 and 2 are made of the same materials and can be made at the same time during the fabrication of a monolithic CMOS integrated circuit.

Figure 6A is a table summarizing the elements of the waveguide and light scattering element of Figure 6 and the CMOS transistor of Figure 1 formed from the same materials at the same time on the same substrate.

One particularly advantageous aspect of the present invention is the use of the salicide blocking layer 3, which is part of the standard CMOS process, as an element of the cladding for the waveguide 650 and the light scattering element 655. The salicide blocking layer 3 is an essential layer in the CMOS process of forming the ohmic contacts needed to make electrical connections to the transistor 160. The salicide blocking layer 3 prevents the deposition of cobalt silicide in any part of a CMOS integrated circuit, where it is not needed. If cobalt silicide is deposited into the core of an optical waveguide, light will not be able to pass through that section of the waveguide. Thus, salicide blocking layer 3 is essential to protecting the core of an optical waveguide from the light blocking deposition of metallic cobalt silicide.

A particularly advantageous aspect of the present invention is the fabrication of the parts of a light scattering element and the elements of a CMOS transistor at the same time and using the same materials on the same substrate, during standard CMOS processing steps.

Figure 7 is a side view, not to scale, of a waveguide with a light scattering element, according to one embodiment of the present invention. Optical waveguide 750 and light scattering element 755 are part of integrated circuit 700, which has been fabricated on substrate 40. Substrate 40 is made of dielectric layer 44, which is typically silicon dioxide and silicon layer 43. On top of silicon dioxide layer 44 is silicon layer 45. Layers 45, 44 and 43 together form what is commonly referred to as a SOI (silicon on insulator) wafer, which is frequently used for the production of CMOS integrated circuits.

Waveguide 750 is made of silicon core 751 and surrounding layers of cladding. The silicon core 751 in a cross sectional view can have one of many possible shapes, such as those of a square, a rectangle, a trapezoid or other form. Silicon dioxide layer 44 functions as a bottom cladding for the core 751. Sidewall passivation layers and sections of field oxide, not shown in Figure 7, are made of dielectric materials and provide side cladding for the waveguide core 751. Sidewall passivation can be formed by thermal oxidation of silicon.

Light scattering element 755 is formed in the silicon core 751 and covered by cladding. Light scattering element 755 can be formed in a variety of manners, such as by etching. Light scattering element 755 includes sidewall passivation layers 1 and field oxide section 15. Sidewall passivation layers 1 and field oxide 15 are typically made of silicon dioxide.

Field oxide 15 is preferably formed in such a manner as to be level with the top of the silicon core 751.

Light scattering element 755 in a cross sectional view can have one of many possible shapes, such as those of a square, a rectangle, a trapezoid or other form. The size and shape of light scattering element 755 is dependent on the requirements of a particular application and is well known to those skilled in the art.

On top of the waveguide core 751 and the light scattering element 755 are dielectric layers 2, 3, 4 and 5, which provide top cladding for the waveguide core 751 and the light scattering element 755. Layer 2 is an oxide spacer layer of dielectric material, typically silicon dioxide. Layer 3 is a salicide blocking layer of dielectric material, typically silicon nitride. Layer 4 is a contact punch-through layer of dielectric material, which can be deposited from a mixture of silicon, oxygen and nitrogen. Layer 5 is an inter-layer dielectric (ILD) which can be made of multiple layers of dielectric material. ILD layer 5 can be made of silicon dioxide or preferably, a low k dielectric, such as silicon carbon oxide.

Light 60 propagating through waveguide core 751 will be mainly confined to the core 751, primarily in a single mode, due to the large difference in refractive indices between the silicon core 751 and the surrounding claddings. The single mode distribution of light propagating in the core 751 is shown by graph 61, which shows that the peak power level of the light in the waveguide 750 is primarily near to the center of the core 751. Graph 61 is an approximate illustration of the distribution of power in the waveguide 750. The silicon core 751 has a refractive index ( $n$ ) of

approximately 3.5 as compared to a refractive index of about 1.5 for silicon dioxide, which is the primary material of the claddings.

As light 60 travels through the waveguide 750 it is primarily confined near to the center of the core, but when the light reaches the boundary with the light scattering element 755, some of the light is scattered downward 63 and some is scattered upward 62. The scattering of light by the light scattering element 755 is primarily due to the abrupt change in refractive index at the boundary between the silicon core 751 and the dielectric materials in the light scattering element 755. The light scattering element 755 includes sidewall passivation layers 1 and the field oxide 15, which are both typically made of silicon dioxide. Monocrystalline silicon has a refractive index of about 3.5, whereas silicon dioxide has a refractive index of about 1.5.

The light scattering element 755, if it is part of a grating coupler, can provide an optical coupling between the core 751 and the layers above and below the core.

Light can also travel in the opposite direction through the light scattering element 755, so that light which is propagating down from a higher level can be coupled into the core of the waveguide by the light scattering element 755.

A typical integrated circuit 700 will have several metal layers above the dielectric layers 5 to provide for interconnections between the components fabricated on the same substrate, but these layers are not shown in Figure 7. For light to be scattered up out of waveguide 750 or for light to be coupled into waveguide 750 from above, there cannot be any segments or pieces of any metal layers directly above the light scattering element 755.

An optical device, such as a grating coupler can be made by forming multiple light scattering elements 755 in the core of a waveguide. Designing such a grating coupler will require, among other things, determining the number, shape, size and spacing of the elements and such design is well known to those skilled in the art.

Many parts or elements of the light scattering element 755 of Figure 7 and the CMOS transistor 160 of Figures 1 and 2 are made of the same materials and can be made at the same time during the fabrication of a monolithic CMOS integrated circuit.

Figure 7A is a table summarizing the parts of the waveguide and light scattering element 755 of Figure 7 and the CMOS transistor of Figure 1 formed from the same materials at the same time on the same substrate.

Silicon layer 45 is used to form the silicon core 751 and the silicon body 161 of CMOS transistor 160 of Figure 1. These silicon elements can be formed of the same material at the same time during the fabrication of a monolithic CMOS integrated circuit.

Light scattering element 755 can be formed by a variety of methods, such as by etching into silicon layer 45. Light scattering element 755 and a trench around the silicon body of the CMOS transistor 160 in Figure 1 can be formed at the same time on the same substrate.

Sidewall passivation layers 1 of the light scattering element 755 and the sidewall passivation layers 1 for the silicon body of CMOS transistor 160 in Figure 1 can be formed at the same time of the same dielectric material on the same substrate.

Field oxide section 15 in the light scattering element 755 and the field oxide 15 surrounding the body of CMOS transistor 160 of Figure 1 can be

formed at the same time from the same dielectric material on the same substrate.

Dielectric layers 2, 3, 4 and 5 used to form the cladding for the waveguide 750 and the light scattering element 755 and dielectric layers 2, 3, 4 and 5 of CMOS transistor 160 in Figure 1 can be formed at the same time of the same dielectric materials on the same substrate.

One particularly advantageous aspect of the present invention is the use of the salicide blocking layer 3, which is part of the standard CMOS process, as an element of the cladding for the waveguide 750 and the light scattering element 755. The salicide blocking layer 3 is an essential layer in the CMOS process of forming the ohmic contacts needed to make electrical connections to the transistor 160. The salicide blocking layer 3 prevents the deposition of cobalt silicide in any part of a CMOS integrated circuit, where it is not needed. If cobalt silicide is deposited into the core of an optical waveguide, light will not be able to pass through that section of the waveguide. Thus, salicide blocking layer 3 is essential to protecting the core of an optical waveguide from the light blocking deposition of metallic cobalt silicide.

A particularly advantageous aspect of the present invention is the fabrication of the parts of a light scattering element and the elements of a CMOS transistor at the same time and using the same materials on the same substrate, during standard CMOS processing steps.

Figure 8 is a side view, not to scale, of a strip loaded waveguide with a light scattering element, according to one embodiment of the present invention. Optical waveguide 850 and light scattering element 855 are part of integrated circuit 800, which has been fabricated on substrate 40.



Substrate 40 is made of dielectric layer 44, which is typically silicon dioxide and silicon layer 43. On top of silicon dioxide layer 44 is silicon layer 45. Layers 45, 44 and 43 together form what is commonly referred to as a SOI (silicon on insulator) wafer, which is frequently used for the production of CMOS integrated circuits.

Waveguide 850 is made of core 851 and surrounding layers of cladding. Core 851 is made of silicon slab 852, dielectric layer 6 and polysilicon strip 9. Silicon slab 852 is formed from silicon layer 45. Polysilicon strip 9 in a cross sectional view can have one of many possible shapes, such as those of a square, a rectangle, a trapezoid or other form. Silicon dioxide layer 44 functions as a bottom cladding for the core 851. Sidewall passivation layers and sections of field oxide on the sides of silicon slab 852, not shown in Figure 8, are made of dielectric materials and provide side cladding for the silicon slab 852. Sidewall passivation can be formed by thermal oxidation of silicon.

Light scattering element 855 is formed in the core 851. Light scattering element 855 includes sidewall passivation layers 7, dielectric layers 8 and dielectric layers 2, 3, 4 and 5, which also function as cladding. Sidewall passivation layers 7 and dielectric layers 8 are typically made of silicon dioxide.

Light scattering element 855 in a cross sectional view can have one of many possible shapes, such as those of a square, a rectangle, a trapezoid or other form. The size and shape of light scattering element 855 is dependent on the requirements of a particular application and is well known to those skilled in the art.

On top of the waveguide core 851 and the light scattering element 855 are dielectric layers 2, 3, 4 and 5, which provide cladding for the waveguide core 851 and the light scattering element 855. Layer 2 is an oxide spacer layer of dielectric material, typically silicon dioxide. Layer 3 is a salicide blocking layer of dielectric material, typically silicon nitride. Layer 4 is a contact punch-through layer of dielectric material, which can be deposited from a mixture of silicon, oxygen and nitrogen. Layer 5 is an inter-layer dielectric (ILD) which can be made of multiple layers of dielectric material. ILD layer 5 can be made of silicon dioxide or preferably, a low k dielectric, such as silicon carbon oxide.

Light 60 propagating through waveguide core 851 will be mainly confined to the core 851, primarily in a single mode, due to the large difference in refractive indices between the core 851 and the surrounding claddings. The single mode distribution of light propagating in the core 851 is shown by graph 61, which shows that the peak power level of the light in the waveguide 850 is primarily near to the center of the core 851. Graph 61 is an approximate illustration of the distribution of power in the waveguide 850.

As light 60 travels through the waveguide 850 it is primarily confined near to the center of the core, but when the light reaches the boundary with the light scattering element 855, some of the light is scattered downward 63 and some is scattered upward 62. The scattering of light by the light scattering element 855 is primarily due to the abrupt change in refractive index at the boundary between the polysilicon strip 9 and the dielectric materials in the light scattering element 855. The light scattering element 855 includes sidewall passivation layers 1 and the field oxide 15, which are

both typically made of silicon dioxide. Monocrystalline silicon has a refractive index of about 3.5, whereas silicon dioxide has a refractive index of about 1.5.

The light scattering element 855 provides an optical coupling between the core 851 and the layers above and below the core.

Light can also travel in the opposite direction through the light scattering element 855, so that light which is traveling down from a higher level can be optically coupled into the core of the waveguide by the light scattering element 855.

A typical integrated circuit 800 will have several metal layers above the dielectric layers 5 to provide for interconnections between the components fabricated on the same substrate, but these layers are not shown in Figure 8. For light to be scattered up out of waveguide 850 or for light to be coupled into waveguide 850 from above, there cannot be any segments or pieces of any metal layers directly above the light scattering element 855.

An optical device, such as a grating coupler can be made by forming multiple light scattering elements 855 in the core of a waveguide. Designing such a grating coupler will require, among other things, determining the number, shape, size and spacing of the light scattering elements and such design is well known to those skilled in the art.

Many parts or elements of the light scattering element 855 of Figure 8 and the CMOS transistor 160 of Figures 1 and 2 are made of the same materials and can be made at the same time during the fabrication of a monolithic CMOS integrated circuit.

Figure 8A is a table summarizing the parts of the waveguide and light scattering element 855 of Figure 8 and the CMOS transistor of Figure 1 formed from the same materials at the same time on the same substrate.

Silicon layer 45 is used to form silicon slab 852 and the silicon body 161 of CMOS transistor 160 of Figure 1. These silicon elements can be formed of the same material at the same time during the fabrication of a monolithic CMOS integrated circuit.

Sidewall passivation layers 7 of the light scattering element 855 and the sidewall passivation layers 7 for the polysilicon gate of CMOS transistor 160 in Figure 1 can be formed at the same time of the same dielectric material on the same substrate.

Dielectric layers 8 of the light scattering element 855 and the dielectric layer 8 which is part of the gate spacer of the CMOS transistor 160 in Figure 1 can be formed at the same time from the same dielectric material on the same substrate.

Dielectric layers 2, 3, 4 and 5 used to form the cladding for the waveguide 850 and the light scattering element 855 and dielectric layers 2, 3, 4 and 5 of CMOS transistor 160 in Figure 1 can be formed at the same time of the same dielectric materials on the same substrate.

In an alternate embodiment of the present invention, light scattering element 855 is formed in a strip loaded waveguide, which does not have a dielectric layer 6, where the polysilicon strip 9 is formed on top of silicon slab 852.

One particularly advantageous aspect of the present invention is the use of the salicide blocking layer 3, which is part of the standard CMOS process, as an element of the cladding for the waveguide 850 and the light

scattering element 855. The salicide blocking layer 3 is an essential layer in the CMOS process of forming the ohmic contacts needed to make electrical connections to the transistor 160. The salicide blocking layer 3 prevents the deposition of cobalt silicide in any part of a CMOS integrated circuit, where it is not needed. If cobalt silicide is deposited into the core of an optical waveguide, light will not be able to pass through that section of the waveguide. Thus, salicide blocking layer 3 is essential to protecting the core of an optical waveguide from the light blocking deposition of metallic cobalt silicide.

A particularly advantageous aspect of the present invention is the fabrication of the parts of a light scattering element and the parts of a CMOS transistor at the same time and using the same materials on the same substrate, during standard CMOS processing steps.

Figure 9 is a side view, not to scale, of a strip loaded waveguide with a light scattering element, according to another embodiment of the present invention. Optical waveguide 950 and light scattering element 955 are part of integrated circuit 900, which has been fabricated on substrate 40. Substrate 40 is made of dielectric layer 44, which is typically silicon dioxide and silicon layer 43. On top of silicon dioxide layer 44 is silicon layer 45. Layers 45, 44 and 43 together form what is commonly referred to as a SOI (silicon on insulator) wafer, which is frequently used for the production of CMOS integrated circuits.

Waveguide 950 is made of core 951 and surrounding layers of cladding. Core 951 is made of silicon slab 952, dielectric layer 6 and polysilicon strip 9. Polysilicon strip 9 in a cross sectional view can have one of many possible shapes, such as those of a square, a rectangle, a trapezoid

or other form. Silicon dioxide layer 44 functions as a bottom cladding for the core 951.

Light scattering element 955 is formed in the core 951, primarily in the silicon slab 952. Light scattering element 955 includes sidewall passivation layers 1 and is filled in by field oxide 15. Sidewall passivation layers 1 and field oxide 15 are typically made of silicon dioxide. Sidewall passivation can be formed by thermal oxidation of silicon.

Light scattering element 955 in a cross sectional view can have one of many possible shapes, such as those of a square, a rectangle, a trapezoid or other form. The design of light scattering element 955, such as its size and shape, is dependent on the requirements of a particular application and is well known to those skilled in the art.

On top of the waveguide core 951 are dielectric layers 2, 3, 4 and 5, which provide side and top cladding for the waveguide core 951. Layer 2 is an oxide spacer layer of dielectric material, typically silicon dioxide. Layer 3 is a salicide blocking layer of dielectric material, typically silicon nitride. Layer 4 is a contact punch-through layer of dielectric material, which can be deposited from a mixture of silicon, oxygen and nitrogen. Layer 5 is an inter-layer dielectric (ILD) which can be made of multiple layers of dielectric material. ILD layer 5 can be made of silicon dioxide or preferably, a low k dielectric, such as silicon carbon oxide.

Light 60 propagating through waveguide core 951 will be mainly confined to the core 951, primarily in a single mode, due to the large difference in refractive indices between the core 951 and the surrounding claddings. The single mode distribution of light propagating in the core 951 is shown by graph 61, which shows that the peak power level of the light in

the waveguide 950 is primarily near to the center of the core 951. Graph 61 is an approximate illustration of the distribution of power in the waveguide 950.

As light 60 travels through the waveguide 950 it is primarily confined near to the center of the core, but when the light reaches the boundary with the light scattering element 955, some of the light is scattered downward 63 and some is scattered upward 62. The scattering of light by the light scattering element 955 is primarily due to the abrupt change in refractive index at the boundary between the silicon slab 952 and the dielectric materials in the light scattering element 955. The light scattering element 955 includes sidewall passivation layers 1 and the field oxide 15, which are both typically made of silicon dioxide. Monocrystalline silicon has a refractive index of about 3.5, whereas silicon dioxide has a refractive index of about 1.5.

The light scattering element 955 provides an optical coupling between the core 951 and the layers above and below the core.

Light can also travel in the opposite direction through the light scattering element 955, so that light which is propagating down from a higher level can be optically coupled into the core 951 of the waveguide by the light scattering element 955.

A typical integrated circuit 900 will have several metal layers above the dielectric layers 5 to provide for interconnections between the components fabricated on the same substrate, but these layers are not shown in Figure 9. For light to be scattered up out of waveguide 950 or for light to be coupled into waveguide 950 from above, there cannot be any segments or pieces of any metal layers directly above the light scattering element 955.

An optical device, such as a grating coupler can be made by forming multiple light scattering elements 955 in the core of a waveguide. Designing such a grating coupler will require, among other things, determining the number, shape, size and spacing of the elements and such design is well known to those skilled in the art.

Many parts or elements of the light scattering element 955 of Figure 9 and the CMOS transistor 160 of Figures 1 and 2 are made of the same materials and can be made at the same time during the fabrication of a monolithic CMOS integrated circuit.

Figure 9A is a table summarizing the parts of the waveguide and light scattering element of Figure 9 and the CMOS transistor of Figure 1, formed from the same materials at the same time on the same substrate.

Silicon layer 45 is used to form the silicon slab 952 of the core 951 and the silicon body 161 of CMOS transistor 160 of Figure 1. These silicon elements can be formed of the same material at the same time on the same substrate.

Sidewall passivation layers 1 of the light scattering element 955 and the sidewall passivation layers 1 for the silicon body 161 of CMOS transistor 160 in Figure 1 can be formed at the same time of the same dielectric material on the same substrate.

Field oxide 15 of the light scattering element 955 and the field oxide 15 around the silicon body 161 of CMOS transistor 160 in Figure 1 can be formed at the same time of the same dielectric material on the same substrate.



Dielectric layer 6 of light scattering element 955 and dielectric layer 6 of the CMOS transistor in Figure 1 can be formed at the same time of the same dielectric material on the same substrate.

Polysilicon strip 9 of light scattering element 955 and polysilicon strip 9 of CMOS transistor in Figure 1 can be formed at the same time of the same material on the same substrate.

Dielectric layers 2, 3, 4 and 5 used to form the cladding for the waveguide 950 and the light scattering element 955 and dielectric layers 2, 3, 4 and 5 of CMOS transistor 160 in Figure 1 can be formed at the same time of the same dielectric materials on the same substrate.

In an alternate embodiment of the present invention, light scattering element 955 is formed in a strip loaded waveguide, which does not have a dielectric layer 6, where the polysilicon strip 9 is formed on top of silicon slab 952.

One particularly advantageous aspect of the present invention is the use of the salicide blocking layer 3, which is part of the standard CMOS process, as an element of the cladding for the waveguide 950 and the light scattering element 955. The salicide blocking layer 3 is an essential layer in the CMOS process of forming the ohmic contacts needed to make electrical connections to the transistor 160. The salicide blocking layer 3 prevents the deposition of cobalt silicide in any part of a CMOS integrated circuit, where it is not needed. If cobalt silicide is deposited into the core of an optical waveguide, light will not be able to pass through that section of the waveguide. Thus, salicide blocking layer 3 is essential to protecting the core of an optical waveguide from the light blocking deposition of metallic cobalt silicide.

A particularly advantageous aspect of the present invention is the fabrication of the parts of a light scattering element and the elements of a CMOS transistor at the same time and using the same materials on the same substrate, during standard CMOS processing steps.

Figure 10 is a side view, not to scale, of a strip loaded waveguide with a light scattering element, according to one embodiment of the present invention. Light scattering element 1055 and optical waveguide 1050 are part of integrated circuit 1000, which has been fabricated on substrate 50. Substrate 50 is made of dielectric layer 44, which is typically silicon dioxide, silicon layer 43, silicon dioxide layer 42 and silicon layer 41. On top of silicon dioxide layer 44 is silicon layer 45. Layers 45, 44, 43, 42 and 41 together form a wafer, and integrated optical and electronic devices can be formed on such a wafer using standard CMOS processes.

Waveguide 1050 is made of a core 1051 and surrounding layers of cladding. Core 1051 is made of silicon layer 43, dielectric layer 44 and silicon strip 1052. Silicon dioxide layer 42 functions as a bottom cladding for the core 1051. Surrounding silicon strip 1052 on both sides of it, but not shown in Figure 10, are sidewall passivation layers 1 and sections of field oxide 15, which serve as side cladding. Sidewall passivation can be formed by thermal oxidation of silicon.

Light scattering element 1055 is formed in silicon strip 1052. Light scattering element 1055 includes sidewall passivation layers 1 and field oxide 15, which are typically made of silicon dioxide.

Light scattering element 1055 in a cross sectional view can have one of many possible shapes, such as those of a square, a rectangle, a trapezoid or other form. The design of light scattering element 1055, including its size

and shape, is dependent on the requirements of a particular application and is well known to those skilled in the art.

On top of the core 1051 are dielectric layers 2, 3, 4 and 5, which function as top cladding. Layer 2 is an oxide spacer layer of dielectric material, typically silicon dioxide. Layer 3 is a salicide block layer of dielectric material, typically silicon nitride. Layer 4 is a contact punch-through layer of dielectric material, which can be deposited from a mixture of silicon, oxygen and nitrogen. Layer 5 is an inter-layer dielectric (ILD) which can be made of multiple layers of dielectric material.

The materials and processing steps used to fabricate light scattering element 1055 are the same ones described in detail with respect to Figure 7, except that light scattering element 1055 is fabricated on a different substrate.

The operation of light scattering element 1055 in Figure 10 is similar to the operation of light scattering element 755 in Figure 7. Light 61 propagating through the waveguide 1050 is confined primarily to the core 1051 as shown in the power distribution graph 60.

As light 60 travels through the waveguide 1050 it is primarily confined near to the center of the core, but when the light reaches the boundary with the light scattering element 1055, some of the light is scattered downward 63 and some is scattered upward 62. The scattering of light by the light scattering element 1055 is primarily due to the abrupt change in refractive index at the boundary between the silicon slab 1054 and the dielectric materials in the light scattering element 1055. The light scattering element 1055 includes sidewall passivation layers 1 and the field oxide 15, which are both typically made of silicon dioxide. Monocrystalline

silicon has a refractive index of about 3.5, whereas silicon dioxide has a refractive index of about 1.5.

The light scattering element 1055 provides an optical coupling between the core 1051 and the layers above and below the core.

Light can also travel in the opposite direction through the light scattering element 1055, so that light which is propagating down from a higher level can be coupled into the core of the waveguide by light scattering element 1055. The light incident from above on the light scattering element 1055 will be coupled into the waveguide 1050.

A typical integrated circuit 1000 will have several metal layers above the dielectric layers 5 to provide for interconnections between the components fabricated on the same substrate, but these layers are not shown in Figure 10. For light to be scattered up out of waveguide 1050 or for light to be coupled into waveguide 1050 from above, there cannot be any segments or pieces of any metal layers directly above the light scattering element .

The dielectric materials listed herein with respect to Figure 1 are all usable as dielectric materials for the waveguide 1050 shown in Figure 10.

As was discussed with respect to the light scattering element 755 in Figure 7, many parts or elements of the light scattering element 1055 of Figure 10 and the CMOS transistor 160 of Figures 1 and 2 are made of the same materials and can be made at the same time during the fabrication of a monolithic CMOS integrated circuit.

Figure 10A is a table summarizing the parts of the waveguide and light scattering trench of Figure 10 and the CMOS transistor of Figure 1, formed from the same materials at the same time on the same substrate.

One particularly advantageous aspect of the present invention is the use of the salicide blocking layer 3, which is part of the standard CMOS process, as an element of the cladding for the waveguide 1050 and the light scattering element 1055. The salicide blocking layer 3 is an essential layer in the CMOS process of forming the ohmic contacts needed to make electrical connections to the transistor 160. The salicide blocking layer 3 prevents the deposition of cobalt silicide in any part of a CMOS integrated circuit, where it is not needed. If cobalt silicide is deposited into the core of an optical waveguide, light will not be able to pass through that section of the waveguide. Thus, salicide blocking layer 3 is essential to protecting the core of an optical waveguide from the light blocking deposition of metallic cobalt silicide.

A particularly advantageous aspect of the present invention is the fabrication of the parts of a light scattering trench and the parts of a CMOS transistor at the same time and using the same materials on the same substrate, during standard CMOS processing steps.

Figure 11 is a cross sectional view, not to scale, of an active waveguide, according to one embodiment of the present invention. Active waveguide 1180 and the CMOS transistor 160 shown in Figure 1 are part of integrated circuit 1100, which has been fabricated on substrate 40. Substrate 40 is made of dielectric layer 44, which is typically silicon dioxide and silicon layer 43. On top of silicon dioxide layer 44 is silicon layer 45. Layers 45, 44 and 43 together form what is commonly referred to as a SOI (silicon on insulator) wafer, which is frequently used for the production of CMOS integrated circuits.

Active waveguide 1180 is made of core 1181 and surrounding layers of cladding. The core 1181 is made of silicon slab 1182, dielectric layer 6 and polysilicon strip 9. The polysilicon strip 9 in a cross sectional view can have one of many possible shapes, such as those of a square, a rectangle, a trapezoid or other form. Silicon dioxide layer 44 functions as a bottom cladding for the core 1181. On one side of silicon slab 1182 is a layer of sidewall passivation 1 and a section of field oxide 15, which serve as side claddings. Sidewall passivation layer 1 is made of dielectric material, typically silicon dioxide. Sidewall passivation can be formed by thermal oxidation of silicon. A section of field oxide 15 is made of dielectric material, typically silicon dioxide. The sides of the polysilicon strip 9 are covered by sidewall passivation layers 7 and dielectric spacer 8. Dielectric layer 6 and dielectric spacer 8 are typically made of silicon dioxide.

On top of core 1181 are dielectric layers 2, 3, 4 and 5, which function as cladding. Layer 2 is an oxide spacer layer of dielectric material, typically silicon dioxide. Layer 3 is a salicide blocking layer of dielectric material, typically silicon nitride. Layer 4 is a contact punch-through layer of dielectric material, which can be deposited from a mixture of silicon, oxygen and nitrogen. Layer 5 is an inter-level dielectric (ILD) which can be made of multiple layers of dielectric material. An ILD like layer 5 can be made of silicon dioxide, but preferably of a low k dielectric, such as silicon carbon oxide.

Active waveguide 1180 as an electronic device operates as a PIN diode. Silicon slab 1182 includes a well implant, which can be positively or negatively doped. In alternate embodiments, silicon slab 1182 does not include a well implant.

Silicon slab 1182 includes doped region 1185 and oppositely doped region 1186, so if region 1185 is P doped, then region 1186 is N doped. Into region 1185 are placed extension implants 16A and source implant 17A. Into region 1186 are placed extension implants 16B and drain implant 17B. Implants 16A and 17A have the same polarity. Implants 16B and 17B are oppositely charged to implants 16A and 17A.

Ohmic contacts 18, typically of cobalt silicide, are made into the doped regions 1185 and 1186 of the active waveguide 1180. After the ohmic contacts 18 have been formed, layers 4 and 5 can be deposited. Coming through layers 4 and 5 are conductive plugs 19, typically made of tungsten, which connect the ohmic contacts 18 to the metal segments 21A and 21B of the first metal layer 21.

First metal layer 21 (M1) is typically made of copper and connects to the conductive plugs 19 from the active waveguide 1180 and provides electrical connections to other circuits on the integrated circuit 100.

Integrated circuits typically have more than one metal layer, but for purposes of simplifying the diagram, no other metal layers are shown in Figure 11.

Active waveguide 1180 can operate as different types of optoelectronic devices, depending on how it is designed and configured, including such devices as a waveguide phase shifter or an attenuator, and such operation is well known to those skilled in the art.

Active waveguide 1180 can operate as a waveguide phase shifter by forward biasing the PIN diode within it using metal connections 21A and 21B. A voltage applied across active waveguide 1180 can change the free carrier density in the silicon slab 1182, which can alter the refractive index

within the silicon 1182. Altering the refractive index as light propagates through the active waveguide 1180, can cause a phase shift and/or attenuation in the light. An active waveguide 1180 can be designed so that varying the voltage across the PIN diode will primarily change the amount of phase shift in light propagating through the device. Active waveguide 1180 operating as a waveguide phase shifter can be used as part of a Mach-Zehnder interferometer functioning as a light modulator.

In alternate embodiments, the implants 16A, 16B, 17A and 17B can all be of the same polarity, either positively or negatively charged. When the implants are all charged with the same polarity, then the active waveguide 1180, as an electronic device operates as a CMOS resistor. If active waveguide 1180 is fabricated as a resistor and a variable voltage is applied across the device, then the free carrier density in the silicon slab 1182 is altered, which can change the refractive index within the silicon slab 1182. Altering the refractive index as light propagates through the active waveguide 1180, can cause a phase shift and/or attenuation in the light. An active waveguide 1180 can be designed so that varying the voltage across the PIN diode will primarily change the amount of attenuation in the light propagating through the device.

An active waveguide operating as a variable attenuator can function as an adjustable loss element, and such a device is sometimes referred to as a VOA or Viable Optical Attenuator.

Many parts or elements of the active waveguide 1180 and the CMOS transistor 160 of Figures 1 and 2 are made of the same materials and can be made at the same time during the fabrication of a monolithic CMOS integrated circuit.



Figure 11A is a table summarizing the elements of the active waveguide of Figure 11 and the CMOS transistor of Figure 1, formed from the same materials at the same time on the same substrate.

Silicon layer 45 is used to form the silicon slab 1182 of active waveguide 1180 and the silicon body 161 of CMOS transistor 160. These silicon elements can be formed of the same material at the same time during the fabrication of a monolithic CMOS integrated circuit.

Sidewall passivation layer 1 of silicon slab 1182 and sidewall passivation layers 1 of CMOS transistor 160 can be formed at the same time of the same dielectric material on the same substrate.

The field oxide 15 on the side of the silicon slab 1182 and the field oxide 15 which surrounds the silicon body 161 of the CMOS transistor 160 can be formed at the same time from the same dielectric material on the same substrate.

Dielectric layer 6 of the active waveguide 1180 and the gate oxide 6 of CMOS transistor 160 can be formed at the same time of the same dielectric material on the same substrate, during the fabrication of a monolithic CMOS integrated circuit.

Polysilicon strip 9 of the active waveguide 1180 and the polysilicon gate 9 of CMOS transistor 160 can be formed at the same time of the same dielectric material on the same substrate, during the fabrication of a monolithic CMOS integrated circuit.

Sidewall passivation layers 7 of active waveguide 1180 and sidewall passivation layers 7 of CMOS transistor 160 can be formed at the same time from the same dielectric material on the same substrate.

Dielectric layers 8 of active waveguide 1180 and dielectric layers 8 of CMOS transistor 160 can be formed at the same time from the same dielectric material on the same substrate.

If silicon slab 1182 of active waveguide 1180 is to receive a well implant that is N doped, then it and a N doped well implant for the silicon body 161 of a PFET CMOS transistor 160 can be formed at the same time using the same doping material on the same substrate.

If silicon slab 1182 of active waveguide 1180 is to receive a well implant that is P doped, then it and a P doped well implant for the silicon body 161 of an NFET CMOS transistor 160 can be formed at the same time using the same doping material on the same substrate.

If they are of the same polarity, extension implant 16A of the active waveguide 1180 and extension implants 16 of a CMOS transistor 160 can be formed at the same time from the same doping material on the same substrate.

If they are of the same polarity, extension implant 16B of the active waveguide 1180 and extension implants 16 of a CMOS transistor 160 can be formed at the same time from the same doping material on the same substrate.

If they are of the same polarity, source implant 17A of the active waveguide 1180 and source, drain and gate implants 17 of a CMOS transistor 160 can be formed at the same time from the same doping material on the same substrate.

If they are of the same polarity, drain implant 17B of the active waveguide 1180 and source, drain and gate implants 17 of a CMOS

transistor 160 can be formed at the same time from the same doping material on the same substrate.

Ohmic contacts 18 of the active waveguide 1180 and ohmic contacts 18 of CMOS transistor 160 can be formed at the same time from the same material on the same substrate.

Conductive plugs 19 of the active waveguide 1180 and conductive plugs 19 of CMOS transistor 160 can be formed at the same time from the same material on the same substrate.

Dielectric layers 2, 3, 4 and 5 used to form the cladding for the active waveguide 1180 and dielectric layers 2, 3, 4 and 5 of CMOS transistor 160 in Figure 1 can be formed at the same time of the same dielectric material on the same substrate.

In alternate embodiments of the present invention, active waveguide 1180 is fabricated without dielectric layer 6, where the polysilicon strip 9 is disposed on top of the silicon slab 1182.

One particularly advantageous aspect of the present invention is the use of the salicide blocking layer 3, which is part of the standard CMOS process, as an element of the cladding for the active waveguide 1180. The salicide blocking layer 3 is an essential layer in the CMOS process of forming the ohmic contacts needed to make electrical connections to the transistor 160. The salicide blocking layer 3 prevents the deposition of cobalt silicide in any part of a CMOS integrated circuit, where it is not needed. If cobalt silicide is deposited into the core of an optical waveguide, light will not be able to pass through that section of the waveguide. Thus, salicide blocking layer 3 is essential to protecting the core of an optical waveguide from the light blocking deposition of metallic cobalt silicide.

A particularly advantageous aspect of the present invention is the fabrication of the elements of an active waveguide 1180 and the elements of a CMOS transistor 160 at the same time and using the same materials on the same substrate, during standard CMOS processing steps.

Figure 12 is a cross sectional view of an active waveguide, according to another embodiment of the present invention. Active waveguide 1290 and the CMOS transistor 160 shown in Figure 1 are part of integrated circuit 1200, which has been fabricated on substrate 50. Substrate 50 is made of dielectric layer 44, which is typically silicon dioxide, silicon layer 43, silicon dioxide layer 42 and silicon layer 41. On top of silicon dioxide layer 44 is silicon layer 45. Layers 45, 44, 43, 42 and 41 together form a wafer, and integrated optical and electronic devices can be formed on such a wafer using standard CMOS processes.

Waveguide 1290 is made of a core 1291 and surrounding layers of cladding. Core 1291 is made of silicon slab 1292, dielectric layer 1293 and silicon strip 1294. Silicon dioxide layer 42 functions as a bottom cladding for the core 1291. Surrounding silicon strip 1294 on both sides of it are sidewall passivation layers 1 and sections of field oxide 15, which serve as cladding. Sidewall passivation layers 1 and field oxide sections 15 are made of dielectric material, typically silicon dioxide. Sidewall passivation can be formed by thermal oxidation of silicon. Dielectric layer 1293 is typically made of silicon dioxide. The silicon strip 1294 in a cross sectional view can have one of many possible shapes, such as those of a square, a rectangle, a trapezoid or other form.

On top of core 1291 are dielectric layers 2, 3, 4 and 5, which function as cladding. Layer 2 is an oxide spacer layer of dielectric material, typically

silicon dioxide. Layer 3 is a salicide blocking layer of dielectric material, typically silicon nitride. Layer 4 is a contact punch-through layer of dielectric material, which can be deposited from a mixture of silicon, oxygen and nitrogen. Layer 5 is an inter-level dielectric (ILD) which can be made of multiple layers of dielectric material. An ILD like layer 5 can be made of silicon dioxide, but preferably of a low k dielectric, such as silicon carbon oxide.

Active waveguide 1290, as an electronic device, operates as a PIN diode. Silicon slab 1292 includes a well implant, which can be positively or negatively doped. In alternate embodiments, silicon slab 1292 does not include a well implant.

Silicon slab 1292 includes doped region 1295 and oppositely doped region 1296, so if region 1295 is P doped, then region 1296 is N doped. Into region 1295 are placed source implant 17A. Into region 1296 are placed drain implant 17B. Implant 17A is oppositely doped to implant 17B.

Ohmic contacts 18, typically of cobalt silicide, are made into the doped regions 1295 and 1296 of the active waveguide 1290. After the ohmic contacts 18 have been formed, layers 4 and 5 can be deposited. Coming through layers 4 and 5 are conductive plugs 19, typically made of tungsten, which connect the ohmic contacts 18 to the metal segments 21A and 21B of the first metal layer 21.

First metal layer 21 (M1) is typically made of copper and connects to the conductive plugs 19 from the active waveguide 1290 and provides electrical connections to other circuits on the integrated circuit 100.

Integrated circuits typically have more than one metal layer, but for purposes of simplifying the diagram, no other metal layers are shown in Figure 12.

Active waveguide 1290 can operate as various types of optoelectronic devices, depending on how it is designed and configured, including such devices as a waveguide phase shifter or an attenuator, and such operation is well known to those skilled in the art.

Active waveguide 1290 can operate as a waveguide phase shifter by forward biasing the PIN diode within it using metal connections 21A and 21B. A voltage applied across active waveguide 1290 can change the free carrier density in the silicon core 1291, which can alter the refractive index within the core 1291. Altering the refractive index as light propagates through the active waveguide 1290, can cause a phase shift and/or attenuation in the light. An active waveguide 1290 can be designed so that varying the voltage across the PIN diode will primarily change the amount of phase shift in light propagating through the device. Active waveguide 1290 operating as a waveguide phase shifter can be used as part of a Mach-Zehnder interferometer functioning as a light modulator.

In alternate embodiments, the implants 17A and 17B can be of the same polarity, either positively or negatively charged. When the implants are all charged with the same polarity, then the active waveguide 1290, as an electronic device, operates as a CMOS resistor. If active waveguide 1290 is fabricated as a resistor and a variable voltage is applied across the device, then the free carrier density in the core 1291 is altered, which can change the refractive index within the core 1291. Altering the refractive index as light propagates through the active waveguide 1290, can cause a phase shift

and/or attenuation in the light. An active waveguide 1290 can be designed so that varying the voltage across the PIN diode will primarily change the amount of attenuation in the light propagating through the device.

An active waveguide operating as a variable attenuator can function as an adjustable loss element, and such a device is sometimes referred to as a VOA or Viable Optical Attenuator.

Many parts or elements of active waveguide 1290 and the CMOS transistor 160 of Figures 1 and 2 are made of the same materials and can be made at the same time during the fabrication of a monolithic CMOS integrated circuit.

Figure 12A is a table summarizing the elements of the active waveguide of Figure 12 and the CMOS transistor of Figure 1, formed from the same materials at the same time on the same substrate.

Silicon layer 45 is used to form the silicon strip 1294 of active waveguide 1290 and the silicon body 161 of CMOS transistor 160. These silicon elements can be formed of the same material at the same time during the fabrication of a monolithic CMOS integrated circuit.

Dielectric layer 44 is used to form the dielectric layer 1293 of active waveguide 1290 and the dielectric layer 44 under silicon body 161 of CMOS transistor 160. These dielectric materials can be formed of the same material at the same time during the fabrication of a monolithic CMOS integrated circuit.

Sidewall passivation layers 1 of silicon strip 1294 of active waveguide 1290 and sidewall passivation layers 1 of CMOS transistor 160 can be formed at the same time of the same dielectric material on the same substrate.

The field oxide 15 on the sides of silicon strip 1294 and the field oxide 15 which surrounds the silicon body 161 of the CMOS transistor 160 can be formed at the same time from the same dielectric material on the same substrate.

If silicon slab 1292 of active waveguide 1290 is to receive a well implant that is N doped, then it and a N doped well implant for the silicon body 161 of a PFET CMOS transistor 160 can be formed at the same time using the same doping material on the same substrate.

If silicon slab 1292 of active waveguide 1290 is to receive a well implant that is P doped, then it and a P doped well implant for the silicon body 161 of an NFET CMOS transistor 160 can be formed at the same time using the same doping material on the same substrate.

If they are of the same polarity, source implant 17A of the active waveguide 1290 and source, drain and gate implants 17 of CMOS transistor 160 can be formed at the same time from the same doping material on the same substrate.

If they are of the same polarity, drain implant 17B of the active waveguide 1290 and source, drain and gate implants 17 of CMOS transistor 160 can be formed at the same time from the same doping material on the same substrate.

Ohmic contacts 18 of the active waveguide 1290 and ohmic contacts 18 of CMOS transistor 160 can be formed at the same time from the same material on the same substrate.

Conductive plugs 19 of the active waveguide 1290 and conductive plugs 19 of CMOS transistor 160 can be formed at the same time from the same material on the same substrate.



Dielectric layers 2, 3, 4 and 5 used to form the cladding for the active waveguide 1290 and dielectric layers 2, 3, 4 and 5 of CMOS transistor 160 in Figure 1 can be formed at the same time of the same dielectric material on the same substrate.

A particularly advantageous aspect of the present invention is the fabrication of the elements of an active waveguide 1290 and the elements of a CMOS transistor 160 at the same time using the same materials on the same substrate, during standard CMOS processing steps.

One particularly advantageous aspect of the present invention is the use of the salicide blocking layer 3, which is part of the standard CMOS process, as an element of the cladding for the active waveguide 1290. The salicide blocking layer 3 is an essential layer in the CMOS process of forming the ohmic contacts needed to make electrical connections to the transistor 160. The salicide blocking layer 3 prevents the deposition of cobalt silicide in any part of a CMOS integrated circuit, where it is not needed. If cobalt silicide is deposited into the core of an optical waveguide, light will not be able to pass through that section of the waveguide. Thus, salicide blocking layer 3 is essential to protecting the core of an optical waveguide from the light blocking deposition of metallic cobalt silicide.

Figure 13 is a top view, not to scale, of a waveguide coupler, according to an embodiment of the present invention. Figure 13 is a simplified view of a waveguide coupler. The various layers of cladding are not shown in Figure 13. Waveguide core 1320 is disposed on top of waveguide core 1310. The shaped end of waveguide core 1310 can direct some of the light 1360 traveling in core 1310 upward into core 1320. Similarly, the shaped end of waveguide core 1320 can direct some of the

light traveling upward from core 1310 sideways into core 1320 as light 1361. Light can travel from left to right, as shown in figure 13 or from right to left through the coupling. Core 1310 can be made of monocrystalline silicon and core 1320 can be made of polysilicon. The shaped ends of cores 1310 and 1320 can have any of a variety of regular or irregular shapes. The core 1320 is fully supported along its length by dielectric material, such as field oxide, except where it is on top of the silicon core 1310. The width of core 1310 as compared to the width of core 1320 can be either wider or narrower, depending on the design for a particular application.

In alternate embodiments, core 1310 does not have a shaped end, but continues under core 1320 to form a polysilicon strip loaded silicon waveguide. The core 1310 can also widen as it continues under the polysilicon strip.

Figure 14 is a block diagram summarizing the process of designing a metal and dielectric stack for an optoelectronic integrated circuit. The process of fabricating an integrated circuit encompasses many steps and diverse materials. The process steps and materials have to be selected in order to make a specific integrated circuit, which will meet its design specifications. The selection of fabrication materials and steps for electronic integrated circuits requires considerable expertise and skill, but has been done for several decades and as a result, is well known to those skilled in the art.

The selection of fabrication materials and process steps for optoelectronic integrated circuits is a relatively new field and many aspects of this process are either not well known or have yet to be discovered. Integrated optoelectronic circuits typically have some combination of

optical, electronic and optoelectronic devices and components. CMOS integrated circuits are typically made of many layers, primarily consisting of devices and components made within the top silicon layer and many layers on top of the active silicon layer. The layers on top of the silicon layer typically include several metal layers and many layers of dielectric materials.

One of the design requirements for optoelectronic circuits which couple light through the top surface of a chip, such as the devices shown in figures 4 to 10 herein, is to optically design the stack of metal and dielectric layers. Metal layers can extend into the area of a stack on a chip, where light must pass through the stack. The design of such a stack in an optoelectronic circuit has to be optimized to maximize the transmission of light through the stack and to minimize the generation of reflections by the layers in the stack.

Figure 14 is a summary in block diagram form of an embodiment of the design process for a metal and dielectric stack. In block 1410, the electrical and optical requirements for the design of a stack of metal and dielectric layers are determined. In block 1420, the metal and dielectric layers for a stack are selected. In block 1430, the selected stack is modeled as a unit. In block 1440, the results of the modeling process in block 1430 are compared to the electrical and optical requirements determined in block 1410.

If the model does not meet the criteria determined in block 1410, then flow returns to block 1420 to reselect the stack of metal and dielectric layers and flow proceeds to block 1430 and 1440, as discussed above.

If the model does meet the criteria established in block 1410, then flow proceeds to block 1450, where this part of the design of an integrated circuit is finalized.

The design and layout of integrated electronic circuits is well known to those skilled in the art. The foundries fabricating integrated circuits have design rules which the layout of an integrated circuit must satisfy. A well known design rule is the specification of the minimum feature size that can be reliably fabricated in a particular process. The minimum line width at many foundries at the current time is 0.13 microns. As new processes are developed in the never ending quest to pack more and more transistors of a smaller size onto a chip, the minimum feature size shrinks to a size smaller than what was available.

The design and layout of nanophotonic integrated circuits is involved with the layout of optoelectronic devices that are smaller than the minimum feature size for a particular process such as CMOS. One aspect of the present invention is the design of optoelectronic elements and devices, with dimensions smaller than the minimum feature size of a process.

Another well known design rule for integrated circuits is the layout of all electronic elements and devices on an  $x - y$  orthogonal grid. Typically, all the electronic elements and devices on electronic chips today have square or rectangular shapes. Standard chip layout rules all assume the use of straight lines and sharp right angle bends and the rules do not anticipate the need for curved lines or non-orthogonal bends or intersections.

The design and layout of nanophotonic circuits frequently requires the specification of curved shapes and features. Another aspect of the present invention is the design of optoelectronic elements and devices, with non-

orthogonal bends, intersections and curved geometric features, which are not part of the process design rules established for electronic elements and devices.

A particularly advantageous aspect of the present invention is the fabrication of the elements of optoelectronic devices and the elements of a CMOS transistor at the same time and using the same materials on the same substrate, using standard CMOS processing steps.

In alternate embodiments of the present invention, optoelectronic devices and integrated electronic devices, such as bipolar junction transistors (BJTs) and junction field effect transistors (JFETs) can be formed on the same substrate, using standard foundry processing steps.

Although the present invention has been described in detail, it should be understood that various changes, substitutions and alterations can be made without departing from the spirit and scope of the invention as defined herein. The embodiments described above are to be considered in all respects as illustrative only and not restrictive in any manner.